ABSTARCT OF THE DISCLOSURE

Detection output from a detection circuit 17 is converted to digital detection data D1 and supplied to an AGC circuit AGCC and a noise clamping circuit NCC that are formed by digital circuits. In the AGC circuit AGCC, a digital low pass filter 19 generates DC voltage data D2 from the detection data D1. A digital divider 20 performs division of the DC voltage data D2 by the reference detection level data D3 indicating the detection data level. A digital multiplier multiplies the division results D4 by the detection data D1 to generate multiplication data D5 that is constant irrespective of a variation in the detection data D1. In the noise clamping circuit NCC, a digital comparator 23 compares the size of the preset voltage data D6 and that of the multiplication data D5. A selector circuit 24 selectively outputs preset voltage data D6 or multiplication data D5 to generate signal wave data D_{AF}.